CLAIMS

1. A lateral high-voltage junction device for over voltage protection of an MOS circuit comprising:

a substrate having a first junction region separated from a second junction region by a substrate region;

an MOS gate electrode overlying the substrate region and separated therefrom by a gate oxide layer; and

dielectric sidewall spacers adjacent to opposing sides of the MOS gate electrode and overlying the substrate region,

wherein the substrate region is defined by a uniformly doped region of the substrate between the first junction region and second junction region.

2. The device of claim 1, wherein first and second junction regions comprise a semiconductor material of the same conductivity type.

3. The device of claim 1, wherein the first junction region comprises a semiconductor material of a first conductivity type, and the second junction region comprises a semiconductor material of a second conductivity type.

4. The device of claim 1, wherein the first junction region comprises an anode and the second junction region comprises a cathode, and wherein the anode and the cathode have an opposite conductivity type.

5. The device of claim 1, wherein the substrate region separating first and second junction regions has a lateral width of about 200nm or less.

6. The device of claim 1, wherein the device is configured to support a voltage of greater than about 2.5 volts is across the first and second junction regions.

7. The device of claim 1, wherein the gate electrode is electrically coupled to the substrate.

8. The device of claim 1, wherein a thickness of the gate oxide layer is substantially the same as a gate oxide thickness of the MOS circuit.

9. An input protection circuit comprising:

a voltage supply node and a ground node;

an MOS circuit coupled to the voltage supply node and to the ground node;

a transistor having a first junction region coupled to the voltage supply node, a second junction region coupled to the ground node, and a substrate region between the first and second junction regions;

an MOS gate electrode overlying the substrate region and separated therefrom by a gate oxide layer; and

dielectric sidewall spacers adjacent to opposing sides of the MOS gate electrode and overlying the substrate region,

wherein the substrate region comprises a junction-free semiconductor region between the first and second junction regions.

10. The input protection circuit of claim 9 wherein the transistor functions as a junction diode such that the first junction region comprises a cathode and the second junction region comprises an anode.

11. The input protection circuit of claim 10 wherein the anode and the substrate region comprise a semiconductor material of the same conductivity type.

12. The input protection circuit of claim 10 wherein the transistor comprises a plurality of 1 to N forward biased diodes connected in series, such that the first junction region of the first diode is coupled to the voltage supply node and the second junction region of the Nth diode is coupled to the ground node.

13. The input protection circuit of claim 9 wherein the transistor functions as a lateral bipolar transistor such that the first junction region comprises an emitter and the second junction region comprises a collector.

14. A parallel bipolar transistor for use as a high voltage handling device in an integrated circuit comprising:

a substrate having a first conductivity type;

a source region and a drain region in the substrate and separated by a channel region, the source and drain regions having a second conductivity type; and

a gate electrode overlying the channel region and separated therefrom by a gate dielectric layer,

wherein the channel region extends from the source region to the drain region, and

wherein a junction between the source region and the channel region functions as an emitter and a junction between the drain region and the channel region functions as a collector,

whereby an absence of LDD extension regions in the channel region provides relatively low parasitic MOS capacitance between the channel region and the gate electrode.

15. The transistor of claim 14, wherein the source region is coupled to a signal node of an MOS circuit and the drain region is coupled to a ground node of the MOS circuit.

16. The transistor of claim 15, wherein a thickness of the gate dielectric layer is substantially the same as a gate dielectric thickness of the MOS circuit.

17. The transistor of claim 14, wherein the gate electrode further comprises dielectric sidewall spacers overlying the channel region adjacent to opposing sides of the gate electrode, and wherein the opposing sides of the gate overlie the channel region at a point away from the source and drain regions.

18. The transistor of claim 14, wherein the MOSFET is configured to support a voltage of greater than about 2.5 volts is across the source and drain regions.

19. The transistor of claim 14, wherein the gate electrode is electrically coupled to the substrate.

20. The transistor of claim 14, wherein the channel region is defined by a uniformly doped region of the substrate between the source region and the drain region.